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DESCRIPTION

PLASMA DISPLAY DEVICE AND POWER MODULE

TECHNICAL FIELD

5 The present invention relates to a plasma display device and a power module, and more particularly to a power module which integrates output transistors for driving a plasma display panel (PDP), and a plasma display device comprising this power module.

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BACKGROUND ART

With the recent increase in the size of display devices, demands are being made for a decrease in the thickness of display devices, and various types of flat display devices have been proposed. For example, a matrix panel which displays a digital signal as is, or in other words a gas-discharge panel such as a PDP, and matrix panels such as a DMD (Digital Micromirror Device), an EL display element, a fluorescent display tube, and a liquid crystal display element have been proposed. Of these flat display devices, the gas-discharge panel has entered into practical use as a display device for a large-screen, direct view HDTV (high definition television) for reasons such as: manufacturing is simple, and therefore the screen can be enlarged easily; the gas-discharge panel is self-luminous, and therefore the display quality is high; and the response speed is high.

In a plasma display device, each field (frame) has a plurality of light-emitting blocks (subfields: SF) constituted by a plurality of sustain discharge pulses, and halftones are displayed in accordance with the combination of subfields. The power consumption of the plasma display device depends on the number of light-emitting pulses (sustain discharge pulses, or sustain pulses) contributing to the light emission, and in recent years, applying a power module which integrates power devices for controlling the sustain pulses to the plasma display device has been considered. Accordingly, it has become desirable to provide a power module in which thermal stress can be reduced, enabling an increase in reliability, and a plasma display device comprising such a power module.

Note that a conventional plasma display device and power module, as well as the problems thereof, will be described in detail below with reference to the drawings.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a plasma display device which is capable of reducing thermal stress in a power module, which is a problem encountered during use of the power module, and thereby extending the life of the power module and reducing power consumption. A further object of the present invention is to provide a power module in which thermal stress can be reduced,

enabling an improvement in reliability.

5 A first aspect of the present invention provides a plasma display device comprising a power module having a plurality of power devices, and temperature detecting means installed in the power module. The temperature of the power module is controlled by feeding temperature information detected by the temperature detecting means back to input signal control means.

10 A second aspect of the present invention provides a power module for driving a plasma display panel in accordance with a signal from input signal control means, comprising a plurality of power devices for generating a drive signal for the plasma display panel, and temperature detecting means for detecting the temperature of the power
15 module. The temperature of the power module is controlled by feeding temperature information detected by the temperature detecting means back to the input signal control means.

20 According to the plasma display device of the present invention, thermal stress in the power module, which is a problem encountered during use of the power module, is reduced, and hence the life of the power module can be increased and power consumption can be reduced. According to the power module of the present invention, thermal stress
25 can be reduced, enabling an improvement in reliability.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described below with reference to the attached drawings, in which:

Fig. 1 is a block diagram showing an example of a conventional plasma display device;

5 Fig. 2 is a schematic diagram showing a heat deterioration characteristic (the life of an element) based on Arrhenius' equation;

Fig. 3 is a view showing the disposal of a power device and a thermal detection element serving as
10 background art;

Fig. 4 is a sectional view showing an embodiment of a power module according to the present invention;

Fig. 5 is a block circuit diagram showing an outline of the main parts in an embodiment of a plasma display device
15 according to the present invention;

Fig. 6 is a view showing an example of a power module and a temperature detection circuit in the main parts of the plasma display device shown in Fig. 5;

Fig. 7 is a view showing the relationship between
20 the temperature of the power module that is applied to the plasma display device of the present invention, and the number of sustain pulses;

Fig. 8 is a flowchart illustrating an example of temperature control processing for controlling the
25 temperature of the power module in the plasma display device of the present invention;

Fig. 9 is a view showing an example of the disposal

of power modules in the plasma display device of the present invention;

Fig. 10 is a block circuit diagram showing an outline of the main parts in another embodiment of the plasma display device according to the present invention; and

Fig. 11 is a view illustrating an example of power reduction processing in the plasma display device according to the present invention.

10 BEST MODES FOR CARRYING OUT THE INVENTION

Before describing embodiments of the plasma display device and power module according to the present invention, a conventional plasma display device and a conventional power module of the background art, and the problems related thereto, will be described in detail with reference to the attached drawings (Figs. 1 to 3).

A plasma display device which detects the temperature of a PDP and each driver in order to compensate the display characteristic and prevent heating has been proposed in the prior art (see Japanese Unexamined Patent Application Publication H9-006283, for example).

Fig. 1 is a block diagram showing an example of a conventional plasma display device, which is an example of the plasma display device disclosed in the above Japanese Unexamined Patent Application Publication H9-006283.

As shown in Fig. 1, a conventional plasma display device S₁ comprises a PDP (plasma display panel) 1, an

address driver 3 which applies an address pulse and a write pulse to address electrodes A_1 to A_M on the basis of a control signal S_A from a control circuit 2, an X common driver 4 which applies a write pulse and a sustain pulse to X electrodes X_1 to X_N on the basis of a control signal S_X from the control circuit 2, a temperature detector 5 which detects the temperature of the X common driver 4 and outputs a detection signal, a Y scan driver 6 which applies a scan pulse to Y electrodes Y_1 to Y_N on the basis of a control signal S_{YS} from the control circuit 2, and a Y common driver 7 which applies a sustain pulse to the Y electrodes Y_1 to Y_N via the Y scan driver 6, on the basis of a control signal S_{YC} from the control circuit 2.

The plasma display device S_1 further comprises a temperature detector 8 which detects the temperature of the Y common driver 7 and outputs a detection signal S_{TY} , a panel heating device 9 which heats the PDP 1, a temperature detector 10 which detects the temperature of the PDP 1 and outputs a detection signal S_{TP} , the control circuit 2, which controls driving of the PDP 1 on the basis of a predetermined signal (a dot clock CLK, display data DATA, a vertical synchronizing signal VSYNC, a horizontal synchronizing signal HSYNC, and so on) and control of a micro-computer 90, a voltage conversion portion 40 which converts a high voltage input from a drive high-voltage input portion IN_v into a voltage for each of the pulses applied to the PDP 1, and an EPROM (Erasable and Programmable Read Only Memory)

50 having a drive waveform area 50A, which stores the waveform of each of the pulses applied to the PDP 1 in advance and outputs the waveform of the desired pulse, and a sustain pulse number setting area 50B.

5 The plasma display device S_1 further comprises an in-device ambient temperature detector 60 which detects the interior temperature of the device, a control circuit 71 which controls the display of an LED 70 for issuing warnings, a control circuit 81 which controls the operation
10 of an air cooling device 80, a relay control portion 91 which prohibits the application of high voltage to the voltage conversion portion 40 and control circuit 2, a power consumption detector 92 which detects the power consumption of the entire device, and the micro-computer 90 which
15 controls each portion of the plasma display device. Note that in this constitution, high voltage power for driving each driver is applied to each driver together with the control signals S_A , S_{YS} , S_{YC} , and S_X . Further, the display data DATA are input from the outside through a display data
20 input portion IN.

 The control circuit 2 comprises a display data control portion 11 which time-divides data corresponding to a single frame (field) of the display data DATA into a plurality of subfield data in accordance with control
25 of the dot clock CLK, display data DATA, and micro-computer 90, and outputs the control signal S_A based on these subfield data, and a panel drive control portion 12 which outputs

the control signals S_x , S_{ys} , and S_{yc} in accordance with control of the vertical synchronizing signal VSYNC, horizontal synchronizing signal HSYNC, and the micro-computer 90. Here, the display data control portion 11 and panel drive control portion 12 exchange data required by each other.

The display data control portion 11 comprises frame memories 20, 22 which temporarily store the input display data DATA frame by frame, and a subtractor 21 which is controlled by the micro-computer 90 to correct the number of gray levels in the display data DATA.

The panel drive control portion 12 comprises a scan driver control portion 30 which outputs the control signal S_{ys} on the basis of a scan pulse P_{Ay} included in the subfield data that are corrected by the display data control portion 11, the vertical synchronizing signal VSYNC, and the horizontal synchronizing signal HSYNC, and a shared driver control portion 31 which outputs the control signals S_{yc} and S_x on the basis of the number of sustain pulses P_{xs} and P_{ys} included in the subfield data that are corrected by the display data control portion 11, the vertical synchronizing signal VSYNC, and the horizontal synchronizing signal HSYNC.

The voltage conversion portion 40 comprises a V_a power source portion 41 which generates a high voltage that is applied to the address electrodes A_1 to A_M in order to generate a write pulse P_{Aw} and an address pulse P_{Aa} , on the

basis of a high voltage that is applied from an external high voltage generating device (not shown) via the drive high pressure input portion IN_V , a V_W power source portion 42 which generates a high voltage that is applied to the X electrodes X_1 to X_N in order to generate a write pulse P_{XW} , a V_{SC} power source portion 43 which generates a high voltage that is applied to the Y electrodes Y_1 to Y_N for the purpose of a main address discharge (wall charge storage discharge) during an address period, a V_Y power source portion 44 which generates a high voltage that is applied to the Y electrodes Y_1 to Y_N in order to generate the scan pulse P_{AY} during the address period, and a V_X power source portion 45 which generates high voltage power (an X address voltage V_X) that is applied to the X electrodes X_1 to X_N for the purpose of the main address discharge (wall charge storage discharge) during the address period.

The micro-computer 90 is connected to a reference voltage output portion OUT for a sustain discharge voltage (sustain pulse voltage), and thus controls the external high voltage generating device (not shown) for generating the sustain discharge voltage, whereby the drive high voltage applied from the drive high voltage input portion IN_V is controlled and the sustain discharge voltage is controlled.

Further, a power electronic circuit device which is capable of realizing an increase in output current without lowering the safety and increasing the structural

complexity of a semiconductor switching element used in a motor control inverter circuit or the like has been proposed in the background art (see Japanese Unexamined Patent Application Publication H11-262241, for example).

5 Japanese Unexamined Patent Application Publication H11-262241 discloses an IGBT module having a power device (IGBT: Insulated Gate Bipolar Transistor) and a temperature sensor, and describes a three-phase inverter circuit installed with six temperature sensors. Moreover,
10 Japanese Unexamined Patent Application Publication H11-262241 discloses a power electronic circuit device which is designed to perform current limitation by controlling the rotation speed of a compressor (air-conditioning motor) to ensure that an
15 element-vicinity temperature, detected by a temperature sensor provided in the vicinity of an IGBT chip, and a junction temperature, estimated on the basis of the average output current of the three-phase inverter circuit, do not exceed a maximum allowable temperature.

20 Fig. 2 is a schematic diagram showing a heat deterioration characteristic (element life) based on Arrhenius' equation, and refers, for example, to the life (the threshold value of allowable characteristic change) of a power device.

25 As shown in Fig. 2, the life of a power device (for example, a power MOSFET, IGBT, power diode, or similar) is approximately 10^5 hours when the temperature of the power

device (the environmental temperature in which the power device is used) is 65°C, for example, but falls to approximately 200 hours when the temperature reaches 150°C, and hence it is known that the life of a power device decreases logarithmically in relation to increases in temperature.

Fig. 3 is a view showing the disposal of a power device and a heat detection element serving as background art. In Fig. 3, the reference numeral 100 denotes a power device unit, 101 denotes a power device, and 102 denotes a temperature detection element. Here, for example, the power device 101 is used in a plasma display device for performing a sustain discharge of a PDP. The power device unit 100 comprising a plurality of the power devices 101 is typically disposed in a perpendicular direction to the ground.

As shown in Fig. 3, in the plasma display device of the background art, the plurality of power devices 101 are arranged at predetermined intervals on the power device unit 100, and the temperature detection elements 102 are provided respectively in the vicinity of each power device 101. Here, the power device 101 is an output driver FET or a power driver FET, and accordingly, the temperature detection element 102 is an output driver temperature detection element or a power driver temperature detection element.

As described above, a device which detects the

temperature of the PDP and each driver to compensate the display characteristic and prevent heating has been proposed in the prior art as a plasma display device.

However, in this plasma display device, for example, the power device 101 used to perform the sustain discharge is not modularized, and instead it has been proposed that the plurality of power devices 101 be mounted directly on a radiator, and that the temperature of the power device 101 be detected by the temperature detection element 102 provided in the vicinity of each power device 101.

The plasma display device disclosed in the aforementioned Japanese Unexamined Patent Application Publication H9-006283 compensates the display characteristic and prevents heating by detecting the temperature of the PDP and drivers, but does not achieve an increase in the life of a power module integrating a plurality of power devices, and a reduction in power consumption.

Further, the aforementioned Japanese Unexamined Patent Application Publication H11-262241 discloses a power electronic circuit device in which a power module is constituted by fixing to a metal block a semiconductor chip formed with a power interrupting semiconductor switching element used in a motor control inverter circuit or the like, and which limits the current of the semiconductor switching element on the basis of the element-vicinity temperature, detected by a temperature

sensor provided in the vicinity of the semiconductor chip,
and a quantity of state relating to the current of the
semiconductor switching element. However, the power
electronic circuit device of Japanese Unexamined Patent
5 Application Publication H11-262241 is fundamentally
different to a device for controlling a power module which
integrates power devices in a plasma display device for
performing display by means of a sustain discharge.
Furthermore, the power electronic circuit device of
10 Japanese Unexamined Patent Application Publication
H11-262241 achieves an increase in the output current
without lowering the element safety and increasing the
structural complexity of the device, but does not achieve
an increase in the life of a power module which integrates
15 a plurality of power devices and a reduction in power
consumption in a plasma display device.

Hence in a conventional plasma display device, for
example, it is necessary to design the radiator of a power
device used to perform a sustain discharge in consideration
20 of the heat that is generated when the number of PDP sustain
pulses is greatest, even in the case of a plasma display
device for performing specific display which has a low
display frequency. Moreover, in a conventional plasma
display device, a power module which integrates a plurality
25 of power devices is not used, and hence an increase in the
life of the power module and a reduction in power consumption
are not achieved.

Embodiments of the plasma display device and power module according to the present invention will now be described in detail with reference to the attached drawings.

5 Fig. 4 is a sectional view showing an embodiment of the power module according to the present invention. In Fig. 4, the reference numeral 210 denotes a power module, 201 denotes a power device, 202 denotes a heat detection element, 203 denotes a ceramic element, 204 denotes a solder
10 fillet, 205 denotes a mold sealing resin, 206 denotes an input/output terminal, 207 denotes a substrate, and 208 denotes a radiator.

 As shown in Fig. 4, the power device 201, heat detection element 202, ceramic element 203, and so on are
15 disposed on the substrate 207. Here, the power device 201 is an element such as an IGBT, a power FET, or another power transistor, or a power diode, for example, and is used to perform a sustain discharge on the plasma display panel in the plasma display device, for example. The ceramic
20 element 203 is a ceramic chip component constituting a resistance or condenser, for example, and is connected to a printed circuit on the substrate 207 by the solder fillets 204. Note that the substrate 207 is a metallic substrate made of aluminum, copper, or the like, or a ceramic substrate
25 made of alumina or the like, for example, and thus serves to convey the heat generated by the power device 201 to the radiator 208 effectively. When the substrate 207 is

a metallic substrate, the printed circuit is provided thereon via an insulator layer.

The power module 210 is constituted such that the power device 201, ceramic element 203, heat detecting element 202, and so on disposed on (wired to) the substrate 207 are sealed by the mold sealing resin 205. Here, as shown in Fig. 4, the radiator 208 for performing thermal diffusion is mounted on the substrate 207, but the radiator 208 may be omitted. Further, the heat detecting element 202 is disposed in the vicinity of the power device 201 serving as a heat-generating element, for example, and hence a thermistor, diode, or thermo-electric couple may be applied as the heat detecting element 202. Note that a predetermined number of the input/output terminals 206 is disposed on the periphery of the mold sealing resin 205, for example.

Fig. 5 is a block circuit diagram showing an outline of the main parts in an embodiment of the plasma display device according to the present invention. In Fig. 5, the reference numeral 211 denotes a diode, 212 denotes a power device drive circuit, 221 denotes an input signal control circuit, 222 denotes a temperature detection circuit, 223 denotes a coil, and 1 denotes the PDP. Here, the input signal control circuit 221 corresponds to the control circuit 2 (common driver control portion 31) and the micro-computer 90 of the plasma display device in Fig. 1. Further, the power module 210 of this embodiment

corresponds to the X common driver 4 and Y common driver 7 of the plasma display device in Fig. 1.

As shown in Fig. 5, the power module 210 of this embodiment is installed with the heat detection element 202, such as a thermistor, a diode, or a thermo-electric couple. Temperature information detected by the heat detection element 202 (for example, resistance value change produced by a thermistor, V_F change produced by a diode, or electromotive force change produced by a thermo-electric couple) is detected by the temperature detection circuit 222 provided on the exterior of the power module 210, the power module temperature information is fed back to the input signal control circuit 221 (the micro-computer 90 of Fig. 1), and thus the temperature of the power module 210 is controlled.

Specifically, for example, when the temperature of the power module 210 reaches or exceeds a predetermined value (a solder surface prescribed temperature value T_0 , for example), the output of the power module 210 is blocked.

Fig. 6 is a view showing an example of the power module and temperature detection circuit in the main parts of the plasma display device shown in Fig. 5. In Fig. 6, a thermistor is used as the temperature detection element 202.

The temperature detection circuit 222 is provided on the exterior of the power module 210, and comprises an operational amplifier circuit (op-amp) 2221, and

resistances 2222 to 2224. One end of the thermistor 202 is connected to a reference potential power wire Vcc, and the other end is connected to the positive input terminal of the operational amplifier circuit 2221 and via the
5 resistance 2222 to a low potential power line (GND). Note that the output of the operational amplifier circuit 2221 is fed back to the negative input terminal of the operational amplifier circuit via the resistance 2224, and connected to the low potential power line (GND) via the resistance
10 2223.

With the thermistor 202 and temperature detection circuit 222 (temperature detecting means) shown in Fig. 6, the resistance value of the thermistor 202, which corresponds to the temperature of the power module 210,
15 is detected by the temperature detection circuit 222, and an output voltage V_o of the temperature detection circuit 222 (the output of the operational amplifier circuit 2221) is fed back to the input signal control circuit 221 (micro-computer 90). Here, the constitution of the
20 temperature detection circuit 222 is merely one example thereof, and various circuit constitutions may be applied. Moreover, the temperature detection element 202 may be a diode, thermo-electric couple, or similar device rather than a thermistor, and the constitution of the temperature
25 detection circuit 222 is modified in various ways in accordance with the applied temperature detection element.

Fig. 7 is a view showing the relationship between

a temperature (temperature increase saturation temperature) T_c of the power module applied to the power display device of the present invention, and the number of sustain pulses (the number of PDP sustain pulses).

5 As is shown clearly in Fig. 7, the temperature increase saturation temperature T_c of the power module 210 can be reduced by lowering the number of sustain pulses in the sustain discharge of the PDP 1. In other words, the temperature of the power module 210 can be controlled
10 by the PDP sustain pulse number.

Fig. 8 is a flowchart illustrating an example of processing for controlling the temperature of the power module in the plasma display device of the present invention, and hence illustrating the power module temperature control
15 processing that is performed by the thermistor 202 and temperature detection circuit 222 shown in Fig. 6.

When the power module temperature control processing begins, first, in a step S1, the temperature of the power module 210 is converted into the corresponding
20 output voltage V_o by the power module 210 and temperature detection circuit 222 described above. The process then advances to a step S2, where the temperature increase saturation temperature T_c of the power module 210 is calculated from the voltage V_o in the input signal control
25 circuit 221 (micro-computer 90). Here, calculation (conversion) of the temperature increase saturation temperature T_c of the power module from the voltage V_o is

performed by converting the voltage V_o (the output of the temperature detecting means (temperature information)) into the temperature increase saturation temperature T_c of the power module using a conversion table stored in a storage device in advance, or by calculating the temperature increase saturation temperature T_c of the power module using a coefficient stored in the storage device in advance, for example. Note that semiconductor memory such as a PROM (Programmable Read Only Memory), for example, may be used as the storage device.

Next, in a step S3, the calculated temperature increase saturation temperature T_c of the power module is compared with the predetermined solder surface prescribed temperature value T_o to determine whether or not the former is lower than the latter. If it is determined in the step S3 that the temperature increase saturation temperature T_c of the power module 210 is lower than the solder surface prescribed temperature value T_o ($T_c < T_o$), the process returns to the step S1, and the same processing is repeated. If, on the other hand, it is determined in the step S3 that the temperature increase saturation temperature T_c of the power module 210 is equal to or greater than the solder surface prescribed temperature value T_o ($T_c \geq T_o$), the process advances to a step S4, where image quality adjustment is performed by reducing the number of sustain pulses of the PDP 1. More specifically, by reducing the number of sustain pulses, the amount of heat generated by the power devices

is reduced, thereby lowering the temperature of the power module 210 and thus adjusting the image quality of the displayed image. The process then returns to the step S1.

5 In the process described above, the temperature of the power module 210 is lowered by reducing the number of sustain pulses of the PDP 1, but control to lower the temperature of the power module 210 can also be performed by reducing the voltage level of the sustain discharge of the PDP 1, or reducing the magnitude of the power source
10 current used in the sustain discharge, for example.

Fig. 9 is a view showing an example of the disposal of the power modules in the plasma display device of the present invention. In Fig. 9, the reference numeral 200 denotes a power device unit. The power device unit 200
15 shown in Fig. 9 comprises two power modules 210, 210, but may comprise more power modules.

As shown in Fig. 9, for example, in the plasma display device, the power device unit 200 is typically disposed in a perpendicular direction to the ground, and
20 the temperature detection element 202 is disposed in the upper portion of each power module 210. Here, the power device unit 200 may comprise only one power module 210.

Note that when the power device unit 200 comprises a plurality of the power modules 210, 210, ..., the temperature
25 detection element 202 may be disposed in the upper portion of only the power module provided in the uppermost position. It is believed that the temperature of the power module

disposed in the uppermost position rises by the greatest extent due to heat convection, and hence by detecting the temperature of the power module disposed in the uppermost position, all of the power modules can be controlled.

5 Furthermore, by reducing the number of temperature detecting means (the temperature detection element, temperature detection circuit, and so on), the control operation can be simplified.

10 Fig. 10 is a block circuit diagram showing an outline of the main parts in another embodiment of the plasma display device according to the present invention. In Fig. 10, the reference numeral 220 denotes a temperature detection module, and 224 denotes a temperature detection value setting circuit.

15 As can be seen clearly from a comparison of Figs. 5 and 10, in the plasma display device of this embodiment, the power module 210 is installed with the temperature detection module 220 instead of the temperature detection element 202, and the output of the temperature detection
20 module 220 is fed back to the input signal control circuit 221 (micon 90) via the temperature detection value setting circuit 224, which is provided on the exterior of the power module 210. Note that the temperature detection value setting circuit 224 may be omitted depending on the
25 functions of the temperature detection module 220.

Fig. 11 is a view illustrating an example of power reduction processing in the plasma display device according

to the present invention. In Fig. 11, the ordinate indicates the temperature increase saturation temperature T_c , and the abscissa indicates the time t . Further, the reference symbol L1 denotes a temperature curve when power reduction processing is not performed, and the reference symbols L2 to L4 denote a temperature curve when the power reduction processing of this embodiment is applied.

First, in a case where full-screen black is displayed on the PDP 1 and power reduction processing is not performed, approximately 80W of power, for example, are consumed when full-screen black display is applied to the PDP 1, and the temperature increase saturation temperature T_c of the power module increases over time, exceeding the solder surface prescribed temperature value T_0 and rising toward the saturation temperature as shown by the curve L1 in Fig. 11.

On the other hand, when the temperature of the power module 210 (the temperature increase saturation temperature T_c of the power module) rises beyond the solder surface prescribed temperature value T_0 during application of the power reduction processing of this embodiment, control is performed to hold the temperature of the power module 210 at a fixed level, as shown by the curve L2 in Fig. 11, and when this condition remains unchanged for a predetermined time period (control setting time period) T_2 , as shown by the curve L2, the output of the power module 210 is blocked, thereby entering a low power consumption

mode. As a result, the temperature (T_c) of the power module 210 decreases over time, as shown by the curve L3. In this low power consumption mode, the approximately 80W of power consumed during full-screen black display are reduced to approximately 1W, for example. After the low power consumption mode has been applied continuously for a predetermined time period, or after the temperature (T_c) of the power module has decreased to a predetermined temperature, it is possible to switch back to normal display mode.

Hence in this embodiment, the temperature information that is detected by the temperature detecting means (temperature detection element 202) installed in the power module 210 is fed back to the input signal control circuit 221 (micro-computer 90), and when the temperature (T_c) of the power module 210 increases beyond a predetermined value (the solder surface prescribed temperature value T_0), the temperature T_c of the power module is controlled to a fixed level (T_0). Moreover, when this condition remains unchanged for the predetermined time period (T_2), control is performed to block the output of the power module 210 and enter into the low power consumption mode (L3). In so doing, breakage of the power devices can be avoided, and power consumption can be reduced.

According to each embodiment of the present invention, breakage of the power devices can be avoided during abnormal heat generation, and by performing serial

temperature monitoring, appropriate control can be applied in accordance with the temperature. Further, according to each embodiment of the present invention, thermal stress can be reduced, enabling an increase in the life of the power module, and as a result, the reliability of the plasma display device can be improved.

According to the present invention as described above, it is possible to provide a plasma display device which is capable of reducing thermal stress in a power module, which is a problem encountered during use of the power module, and thereby extending the life of the power module and reducing power consumption. Also according to the present invention, it is possible to provide a power module in which thermal stress can be reduced, enabling an improvement in reliability.